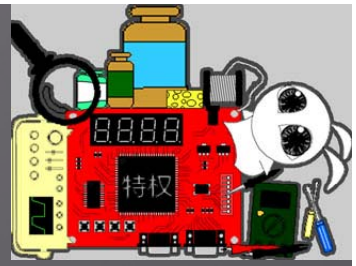
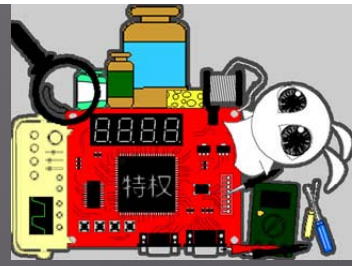
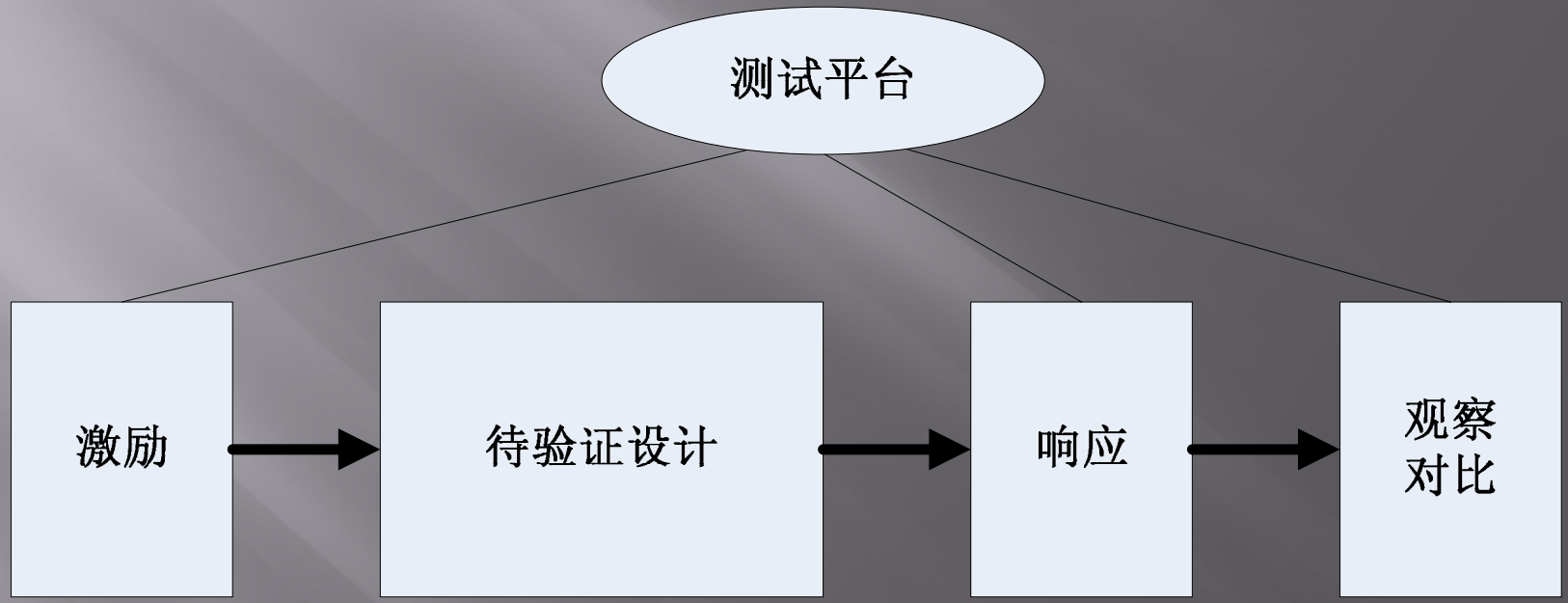
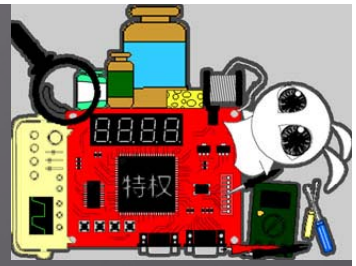


Lesson 8
简单的Testbench设计

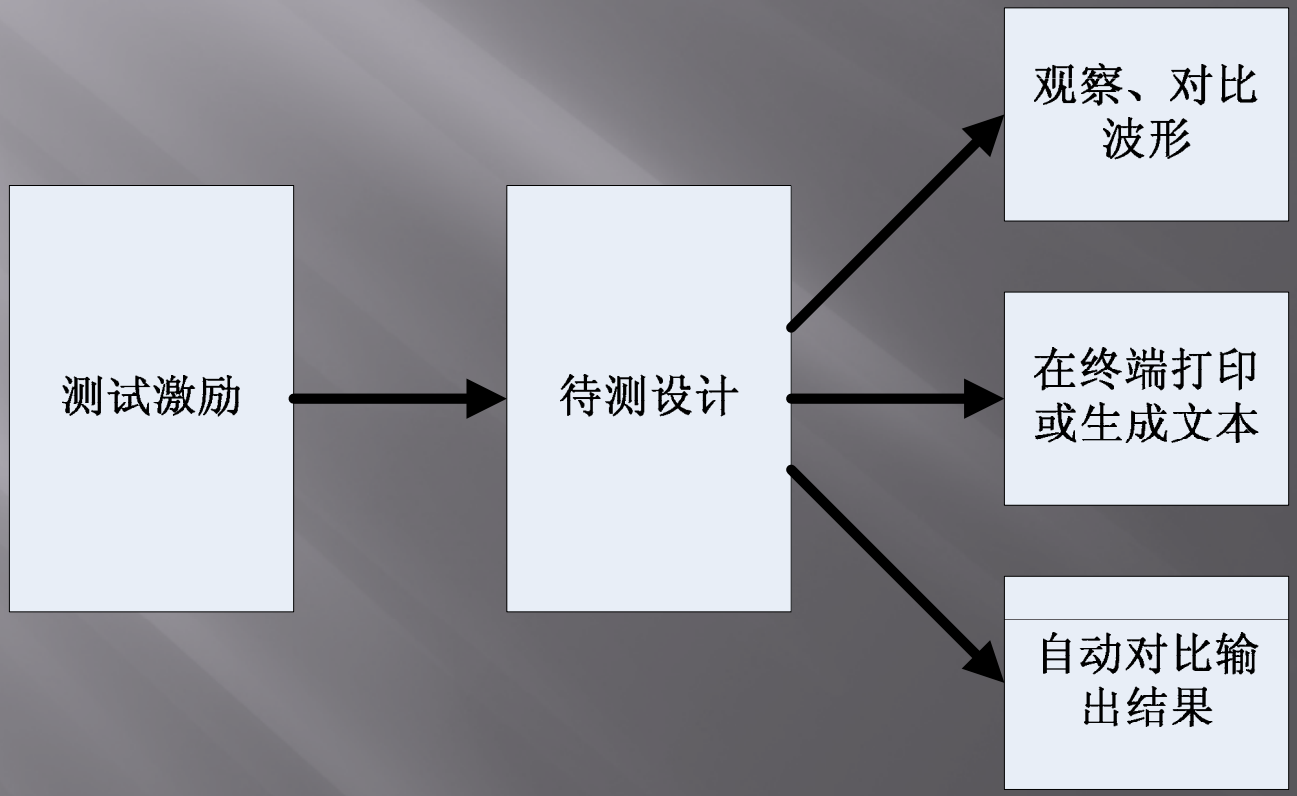


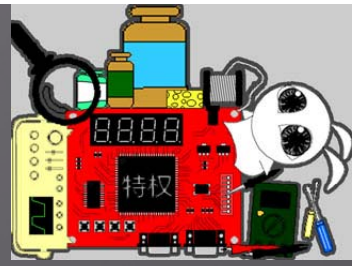
Testbench的基本概念：





Testbench的基本概念：



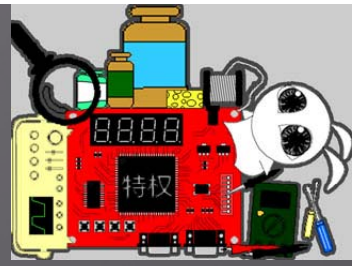


Testbench三步走：

① 对被测试设计的顶层接口进行例化。

② 给被测试设计的输入接口添加激励。

③ 判断被测试设计的输出响应是否满足设计要求。

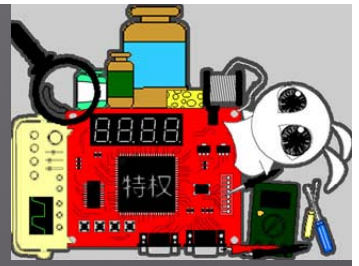


最简单的Testbench：

时钟产生

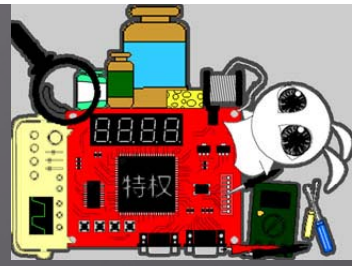
复位产生

其他激励产生



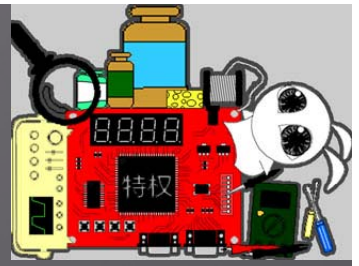
最简单的Testbench：

```
//时钟产生
//定义时钟周期为20ns，已定义“`timescale 1ns/1ps”
parameter PERIOD = 20;

initial begin
        clk = 0;
        forever
                #(PERIOD/2) clk = ~clk;
end
```



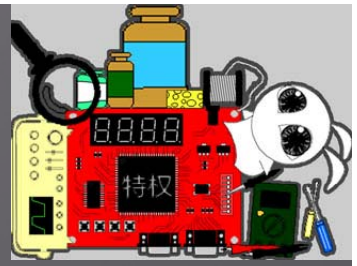
最简单的Testbench：

```
//时钟产生
//定义时钟周期为20ns，已定义“`timescale 1ns/1ps”
parameter PERIOD = 20;

always begin
        #(PERIOD/2) clk = 0;
        #(PERIOD/2) clk = 1;
end
```



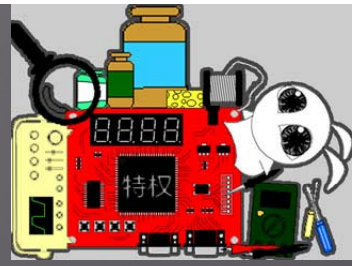
最简单的Testbench：

```
//复位产生
initial begin
        //复位低有效，已定义“`timescale 1ns/1ps”
        rst_n = 0;
        #100;          //100ns延时
        rst_n = 1;     //撤销复位
        ……
end
```



最简单的Testbench：

```
//复位产生
initial begin
        reset_task(100);  //复位100ns，已定义“`timescale 1ns/1ps”
        ……
end

task reset_task;
input[15:0] reset_time;      //复位时间
begin
        reset = 0;
        #reset_time;
        reset = 1;
end
```



好书推荐：

吴继华,王诚《设计与验证Verilog HDL》

Janick Bergeron. 《Writing Testbench》
张春,陈新凯,李晓雯等译《编写测试平台》