寄存器 00：AGC 增益控制
Register 01 - rw: Blue gain control
Register 02 - rw: Red gain control
Register 03 - rw: 饱和度控制
Register 04 & 05 - w: Reserved Register
Register 06 - rw: 亮度控制
Register 07 - rw: Angalog 锐度控制
Register [08] ~ [0B] - w: Reserved.
Register 0C - rw:背景白平衡控制 -蓝色通道
Register 0D - rw: 背景白平衡控制 --红色通道
Register 0E ~ 0F- rw: Reserved
Register 10 - rw: 自动曝光控制寄存器
Register 11 - rw: 时钟速率控制
Register 12 - rw: Common control A
Register 13 - rw: Common control B
Register 14- rw: Common control C
Register 15- rw: Common control D
Register 16 - rw: Frame Drop
Register 17 - rw: 水平窗口启动
Register 18 - rw: 水平窗口结束
Register 19- rw: 垂直窗口启动
Register 1A- rw: 垂直窗口结束
Register 1B- rw: 像素转换
Register 1C- r: 制造 ID 高字节
Register 1D- r: 制造 ID 低字节
Register 1E ~ 1F- rw: Reserved
Register 20- rw: Common control E
Register 21- rw: Y 通道偏移调整
Register 22- rw: U 通道偏移调整
Register 23- rw: 晶体电流控制。
Register 24- rw: AEW 自动曝光白色像素比
Register 25- rw: AEC 自动曝光黑色像素比
Register 26 - rw: Common control F
Register 27 - rw: Common control G
Register 28 - rw: Common control H
Register 29 - rw: Common control I
Register [2A] - rw: 帧速率调整寄存器 1
Register [2B] - rw: 帧速率调整寄存器 2
Register [2C] - rw: Black Expanding Register
Register [2D] - rw: Common Control J
Register [2E]- rw: V 通道偏移调整
Register 2F ~ 5F - w: Reserved
Register 60- rw: 信号处理 Control A
Register 61- rw: 信号处理 Control B

Register 62- rw: RGB Gamma Control
Register 63- rw: Reserved
Register 64- rw: Y Gamma Control
Register 65- rw: 信号处理 Control C
Register 66- rw: AWB 过程控制
Register 67- rw: 颜色空间选择
Register 68- rw: 信号处理 Control D
Register 69- rw: 模拟锐度
Register 6A- rw: 垂直边缘增强控制
Register 6B-6E rw: Reserved
Register 6F - rw: 偶/奇噪声补偿控制
Register 70 - rw: Common Control K
Register 71 - rw: Common Control J
Register 72- rw:水平同步第一边移
Register 73 - rw: 水平同步第二边移
Register 74 - rw: Common Control M
Register 75 - rw: Common Control N
Register 76 - rw: Common Control O
Register 77-7B - rw: Reserved
Register 7C - rw: Field Average Level Storage

寄存器 00：AGC 增益控制

Bits	Null	AGC6	AGC5	AGC4	AGC3	AGC2	AGC1	AGC0
Default	-	-	0	0	0	0	0	0

AGC<5:0> -增益设置为整个图像通道

计算公式为：

Gain = (AGC<3:0>/16+1)*(AGC<4>+1)*(AGC<5>+1); range (1x ~ 7.75x), AGC<5> and AGC<4> control SA2.

Register 01 - rw: Blue gain control

Bits	BLU7	BLU6	BLU5	BLU4	BLU3	BLU2	BLU1	BLU0
Default	1	0	0	0	0	0	0	0

BLU<6:0> - white balance value for the blue channel.
The formula is:
Blue_gain=1+(BLU<7:0> - [80])/[100]; range (0.5x ~ 1.5x).
BLU<7> - Sign bit. If "1", Blue gain increase; "0" gain decrease.

Register 02 - rw: Red gain control

Bits	RED7	RED6	RED5	RED4	RED3	RED2	RED1	RED0
Default	1	0	0	0	0	0	0	0

RED<6:0> - white balance value for the red channel.
The formula is:
Red_gain=1+(RED<7:0> - [80])/[100]; range (0.5x ~ 1.5x).
RED<7> - Sign bit. If "1", Red channel gain increase; "0" gain decrease.

寄存器 3：饱和度控制

Bits	SAT7	SAT6	SAT5	SAT4	SAT3	SAT2	SAT1	SAT0
Default	1	0	-0	0	0	0	0	0

SAT<7:0>-saturation adjustment(饱和度调整) for the UV channel based on the default setting;
范围（-4dB～+6dB）。如果 SAT<7:0>>[80]，增加;若 SAT<7:0><[80]，减少

Register 06- rw:亮度控制

Bits	BRT7	BRT6	BRT5	BRT4	BRT3	BRT2	BRT1	BRT0
Default	1	0	0	0	0	0	0	0

BRT<7:0> -亮度调整为 Y/ RGB 的基础上的默认设置通道;范围（-200mV 的～+200mv）。如果 BRT<7:0>>[80]，亮度增加;如果 BRT<7:0><[80]，亮度减少。该寄存器是自动/手动控制。如果寄存器 2D　bit4 = 1，这个寄存器由芯片控制自动，如果写这个寄存器的值，这个值将被更新内部电路。只有当 2D bit4 =0，这个寄存器可以设置为任意值

Register 07 - **rw:** Angalog 锐度控制　2d

Bits	HS7	HS6	HS5	HS4	HS3	HS2	HS1	HS0
Default	0	0	1	0	1	1	1	1

SHP<7:4> - Sharpness Threshold. 锐度阈值。
SHP<3:0> - Sharpness Magnitude. 锐度震级。

Register 0C - rw: 白平衡控制背景-蓝色通道。

Bits	Null	Null	ABLU5	ABLU4	ABLU3	ABLU2	ABLU1	ABLU0
Default	-	-	1	0	0	0	0	0

ABLU<4:0> -白平衡背景蓝色成分比例的调整。调整分辨率 0.625％，总范围为（20％- -20％），
该寄存器用于抵消图像的背景蓝色构成比
ABLU<5> -符号位。如果“1“，降低背景蓝色的成份比例，“0“蓝色成分的比例增加

Register 0D - rw: White Balance background control -- Red channel

Bits	Null	Null	ARED5	ARED4	ARED3	ARED2	ARED1	ARED0
Default	-	-	1	0	0	0	0	0

Changes AWB Hue Control
ARED<4:0> - White Balance background red color component ratio adjustment. Adjust resolution is 1.5% and total range is (+20% - -20%) This register is used to offset image background red component ratio.
ARED<5> - Sign bit. If “1”, decrease background red component ratio; “0” increase red component ratio.

Register 10 - rw:自动曝光控制寄存器

Bits	AEC7	AEC6	AEC5	AEC4	AEC3	AEC2	AEC1	AEC0
Interlace	0	1	1	1	1	1	1	1
Progres-sive Scan	1	1	1	1	1	1	1	1

AEC<7:0> -曝光时间设定，计算公式为
隔行扫描：$T_{EXPOSURE} = T_{LINE} \times AEC(7:0)$;
逐行扫描：$T_{EXPOSURE} = T_{LINE} \times AEC(7:0)x2$;
T_{LINE} = Frame Time / 525
if use 27MHz, T_{LINE} = 63.5 uS
范围：[00] - [7F] for Interlaced; [00] - [FF] for Progressive Scan.
*只有当设置为手动设置模式时，这个寄存器设置才是有效的（寄存器 13 bit0=0）
如果 13 bit0=1。。。。。。。。。（）

如果寄存器 13 bit0 =0，或寄存器 29 bit7 = 1，寄存器将保持最后一个值不变（无论是从 SCCB 或 AEC 算法的结果输入）。
*在改变这个设置后，到达预期的曝光设置通常需要不少于两个场的时间

Register 11 - rw:时钟速率控制

Bits	SYN7	SYN6	CLK5	CLK4	CLK3	CLK2	CLK1	CLK0
Default	0	0	0	0	0	0	0	0

CLK<5:0> -系统时钟预分频器；这个寄存器定义芯片的像素时钟速率，公式为：
(16 Bit mode) PCLK = (CLK_input / ((CLK<5:0> + 1) * 2))
(8 Bit mode) PCLK = (CLK_input / (CLK<5:0> + 1))
SYN<7:6> - 三同步输出极性选择：
SYN7 = 0, SYN6 = 0: HSYNC negative, CHSYNC negative, VSYNC positive edge;
SYN7 = 0, SYN6 = 1:.HSYNC negative, CHSYNC negative, VSYNC negative;
SYN7 = 1, SYN6 = 0: HSYNC positive, CHSYNC negative, VSYNC positive.
SYN7 = 1, SYN6 = 1: HSYNC negative, CHSYNC positive, VSYNC positive.
*这项改变的效果是立竿见影的，但是，它通常需要对图像约两个场达到稳定状态

Register 12 - rw: Common control A

Bits	COMA7	COMA6	COMA5	COMA4	COMA3	COMA2	COMA1	COMA0
Default	0	0	1	0	0	1	0	0

COMA7 – “1“软启动芯片复位，复位发生后，该芯片初始化为默认状态，所有的寄存器包括 SCCB 的内容设置为默认，此位是自复位后清除。
COMA6 - “1” selects mirror image
COMA5 - “1” 使能 AGC. “0” – 停止 AGC并且设置寄存器[00] 为初始值. 只在自动模式下起作用。
COMA4 - “1”选择 8 位数字输出格式 Y U Y V Y U Y V ...
COMA3 - “1” selects raw data signal as video data output, “0” selects YCrCb as video data output.
COMA2 - “1”使能自动白平衡，“0” AWB stop and AWB register [01] and [02] value is held at last updated value.
COMA1 - “1”选择彩条测试模式输出
COMA0 - “1” select precise A/D Black Level Compensation (BLC) line method. “0” use standard black levelcompensation to do A/D BLC field method which is more stable but less precise.

Register 13 - rw: Common control B

Bits	COMB7	COMB6	COMB5	COMB4	COMB3	COMB2	COMB1	COMB0
Default	-	-	0	0	0	0	0	1

COMB7 - Reserved.

COMB6 - Reserved.

COMB5 - “1”选择8位数据模式，Y/CrCb and RGB，“0”选择16位数据模式，数据go to both **Y<7:0>** bus and **UV<7:0>** bus.

COMB4 - “0”使能数字输出CCIR601格式。“1” 使能CCIR656 格式.

COMB3 - “0”选择水平同步输出**CHSYNC脚** ，“1”选择复合同步输出。

COMB2 - “1” tri-states bus **Y<7:0>** and **UV<7:0>**, “0” enables both buses.

COMB1 - “1” 启动单一帧传输，for this function to work, field drop mode (FD<1:0> in register[16]) must set to “OFF”. 见下图. After this bit is set, for Interlaced mode, **HREF** isonly asserted for consecutive two fields beginning at Odd field. This bit is cleared automaticallyat the end of this frame. For Progressive Scan mode, **HREF** is only asserted for oneframe. Clearing this bit in the middle of active frame has no effect to the assertion of current **HREF**.

COMB0 - “1” 启用自动调整模式，在这种模式下，内部电路将覆盖这些参数曝光在寄存器[00]～[02]，“0”手动调节模式.

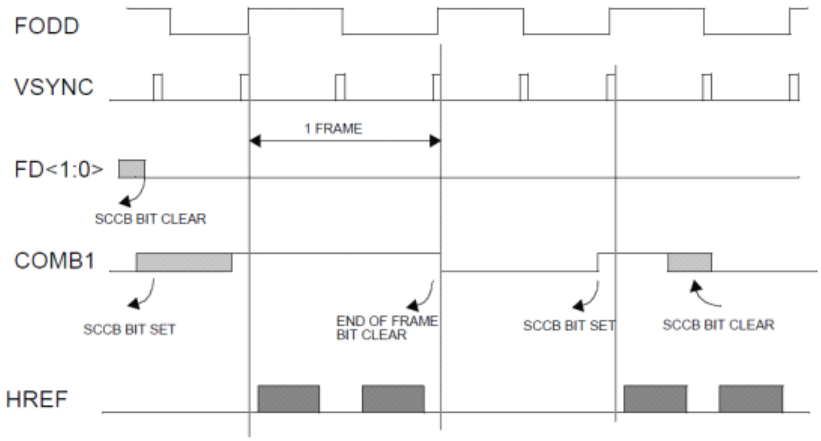


FIG 1.7 Single Frame Transfer Example (Interlaced Mode)

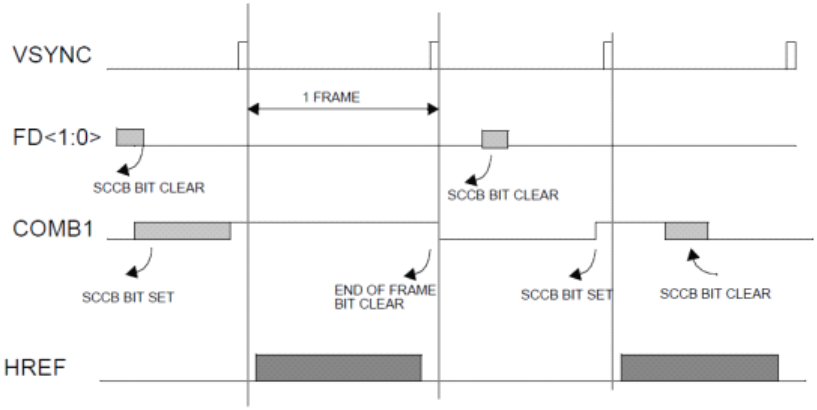


FIG 1.8 Single Frame Transfer Example (Progressive Scan Mode)

Register 14- rw: Common control C

Bits	COMC7	COMC6	COMC5	COMC4	COMC3	COMC2	COMC1	COMC0
Default	0	-	0	0	0	1	-	-

COMC7-AWB 激活阈值的选择：1 -高;0 低。
COMC6- 保留。
COMC5-QVGA 的数字输出格式选择。 **1 -320 × 240;** **0 -640x480 分辨率显示器。**
COMC4-场/帧在垂直同步垂直同步输出端口选择：1 -**帧同步，只在奇数插入**
场垂直同步； 0 -场垂直同步，在隔行扫描模式的影响
COMC3-的 HREF 极性选择：0 –HREF 积极，1 -的 HREF 消极。
COMC2-的 RGB gamma 选择：1- γ，价值定义为寄存器[62]的值，0- γ 为 1（线性）。
COMC1- 保留。
COMC0- 保留。

Register 15- rw: Common control D

Bits	COMD7	COMD6	COMD5	COMD4	COMD3	COMD2	COMD1	COMD0
Default	-	0	-	-	-	-	-	1

COMD7- 保留。
COMD6-PCLK的极性选择。“0“OV7620在PCLK的下降沿输出数据和数据总线将是稳定的在PCLK的上升沿;在PCLK的“1”的上升沿输出数据和稳定的下降沿。当OV7620工作CCIR656格式，COMB4= 1，该位被禁用，而应使用PCLK的上升边沿锁存 数据总线。
COMD<5:1>- 保留。
COMD0- U V digital output序列外汇管制。 0 - V U V U .....为16位，V Y U Y ...8位; 1- U

V U V ...为 16 位和 U Y V Y ...为 8 位。

Register 16 - rw: Frame Drop

Bits	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
Default	0	0	0	0	0	0	1	1

FD<7:2>- **Frame Drop**的选择，it operates in ODD and EVEN mode as defined by FD<1:0>, it is ignored in OFF & FRAME mode。其目的是分裂成视频信号编人数在时隙场/帧单元，并允许被激活的HREF只有一个字段/帧在时期。此功能不会影响或像素的视频数据率。000000 -000001：禁用数字数据输出，只输出黑色参考电平。000010-111111：输出1（2～63）帧。如果设置寄存器33位1= 1，这意味着仅下降1架由（2～63）帧。

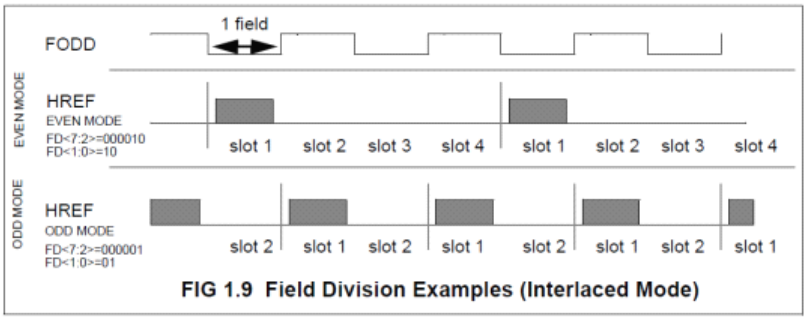


FIG 1.9 Field Division Examples (Interlaced Mode)

隔行:

FD<1:0>- 场模式选择. Each frame consists of two fields: Odd & Even, these bits defines the assertion of HREF in relation to the two fields.

00 - OFF mode; HREF is not asserted in both fields, one exception is the single frame transfer operation (see the description for the register [13])

01 - ODD mode; HREF is asserted in odd field only.

10 - EVEN mode; HREF is asserted in even field only.

11 - FRAME mode; HREF is asserted in both odd field and even field. FD<7:2> useless (default).

寄存器 17：**水平窗口的开始**

Bits	HS7	HS6	HS5	HS4	HS3	HS2	HS1	HS0
Default	0	0	1	0	1	1	1	1

HS<7:0> -选择的 HREF 窗口的出发点，每个 LSB 代表四个交错像素/进全分辨率模式下，两个像素的 QVGA 分辨率模式，此值设置在内部计数器的列，默认值对应于 640 水平的窗口。最大窗口大小为 664。看到窗口下面的说明。HS<7:0>可编程范围是[2C] - [D2]，并应少于 HE<7:0>。HS<7:0>应可编程值大大于或等于[2C]。值大于[D2]是无效的

Register 18 - rw: Horizontal Window end

Bits	HE7	HE6	HE5	HE4	HE3	HE2	HE1	HE0
Default	1	1	0	0	1	1	1	1

选择的 HREF 窗口的终点，每个 LSB 代表四个像素全分辨率和两个像素的 QVGA 分辨率，此值设置基于一个内部列计数器，默认值对应到最后一个可用像素。HE<7:0>的可编程范围为[2D] - [D2 的]。HE<7：0>应大于 HS<7：0>，小于或等于[D2]。值大于[D2 的]是不可以的。

Register 19- rw: Vertical Window start

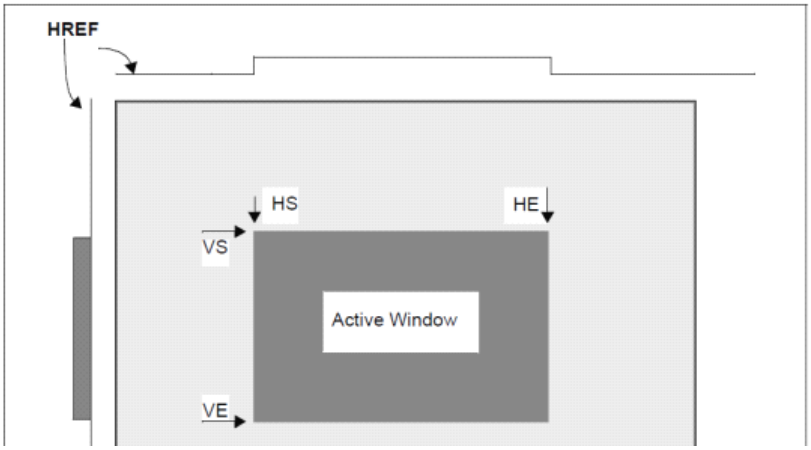
Bits	VS7	VS6	VS5	VS4	VS3	VS2	VS1	VS0
Default	0	0	0	0	0	1	1	0

选择窗口的垂直起始行全分辨率模式下，每个 LSB 代表 1scan 在某一领域线隔行扫描模式，2 个扫描在一帧逐行扫描模式行。在 QVGA 分辨率（设置寄存器 14 位 5），每个 LSB 代表在一个领域 1 次扫描线隔行扫描模式，1scan 在一帧线逐行扫描模式。Min 是[05]，最大。是[F6]，并应小于 VE<7:0>。

Register 1A- rw: Vertical Window end

Bits	VE7	VE6	VE5	VE4	VE3	VE2	VE1	VE0
Default	1	1	1	1	0	1	0	1

VE<7:0>-选择垂直窗口结束排在全分辨率模式下，每个 LSB 代表 1scan 在某一领域线隔行扫描模式，2 个扫描在一帧逐行扫描模式行。在 QVGA 分辨率，每个 LSB 代表一扫描场隔行扫描模式之一，1scan 逐行在一帧逐行扫描方式。Min[5]，最大。是[F6]，并应大于 VS7:0>。



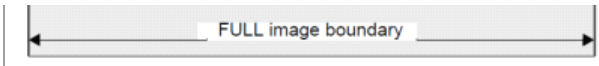


FIG 1.11 Window Sizing

As shown above, HS<7:0> defines the starting pixel within a scan line, HE<7:0> defines the ending pixel within a scan line. VS<7:0> defines the starting row within a field, VE<7:0> defines the ending row within a field. VS/VE automatically defines the window height of a image frame. The rectangular window defined by HS/HE/VS/VE is the active image window. Only pixels insides this window is valid, along with the **HREF** timing signals, black level substitutes the pixel data when outside the active window.Identical value for HS/HE or VS/VE is not permitted since it causes undefined window size.If end point is lower than the starting point, the window begins from the starting point and ends at the far end of the available image boundary.The window size calculate formula is as below:

1. Horizontal size: VGA mode: Horizontal window size = (Register [18] - Register [17])*4.
QVGA mode: Horizontal window size = (Register [18] - Register [17])*2.
2. Vertical size: VGA mode: Vertical window size = (Register [1A]- Register [19]+1);
QVGA mode: Horizontal window size = (Register [1A] - Register [19]+ 1).

Register 1B- rw:像素转换

Bits	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0
Default	0	0	0	0	0	0	0	0

PS<7:0> - to provide a way to fine tune the output timing of the pixel data relative to that of **HREF**, it physically shifts the video data output time early or late in unit of pixel clock as shown in the figure below. This function is different from changing the size of the window as is defined by HS<7:0> & HE<7:0> in register [17] and [18].

The number of pixels that can only be shifted late. Maximum shift pixel number is 255.

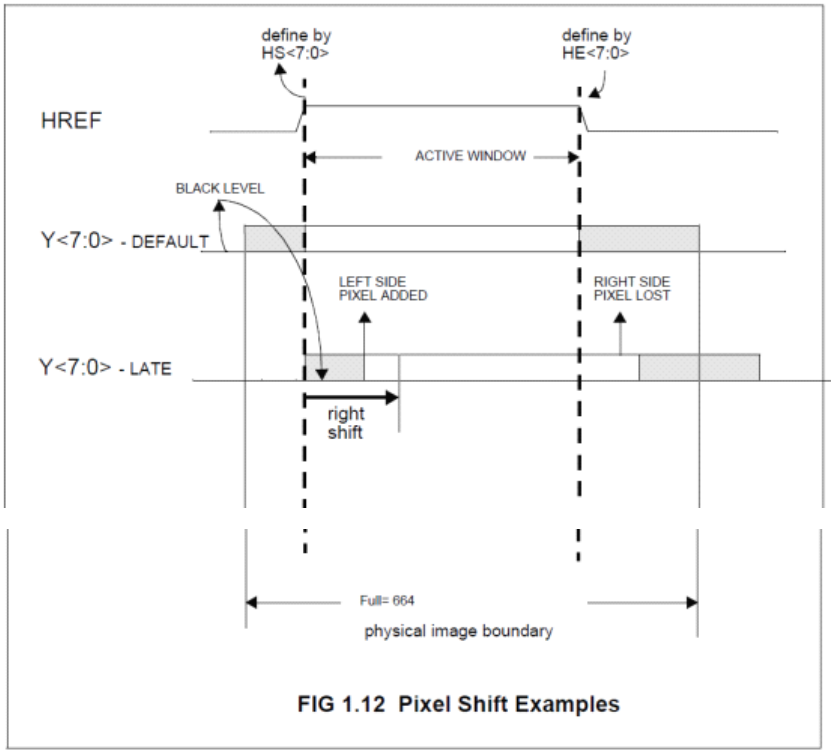


FIG 1.12 Pixel Shift Examples

Register 1C- r: Manufacture ID high byte

Bits	MIDH7	MIDH6	MIDH5	MIDH4	MIDH3	MIDH2	MIDH1	MIDH0
Default	0	1	1	1	1	1	1	1

Register 1D- r: Manufacture ID low byte

Bits	MIDL7	MIDL6	MIDL5	MIDL4	MIDL3	MIDL2	MIDL1	MIDL0
Default	1	0	1	0	0	0	1	0

Register 20- rw: Common control E

Bits	COME7	COME6	COME5	COME4	COME3	COME2	COME1	COME0
Default	0	0	0	0	0	-	0	0

COME1-AWB 快速/低速模式的选择。 “1” -AWB 始终是快速模式，即寄存器[01]和[02]是改变每场/帧。 “0”AWB 是缓慢的模式，[01]和[02]改变每 16/64 场/

70 帧决定通过寄存器位 1。当 AWB 使能，寄存器 12　bit2 = 1，AWB 正在工作，
快速模式起初 1024 场/帧，不是作为低速模式以后。

Register 21- rw: Y 通道偏移调整

Bits	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
Default	1	0	0	0	0	0	0	0

Y6-Y0:Y 通道数字输出偏移调整。范围：127 毫伏～-127mV。如果 COMG2=0 时，该寄存器将自动更新内部的 A / D 背光补偿电路，写一个值到这个 SCCB 寄存器没有任何效果。如果 COMG2= 1，Y 通道偏移调整将使用寄存器中的值它可以改变 SCCB。如果 COMF1= 0，该寄存器没有到 A / D 调整的影响输出数据。如果输出 RGB 原始数据，该寄存器将调整的 R / G/ B 的数据。
Y7: 调整的方向偏移 0 -addY[6:0]　1 -Subtract y[6:0]。

Register 22- rw: U Channel Offset Adjustment

Bits	U7	U6	U5	U4	U3	U2	U1	U0
Default	1	0	0	0	0	0	0	0

U6-U0:U 通道数字输出偏移调整。范围：128 毫伏～-128mV。如果寄存器 27 bit2 =0，这个寄存器会自动更新内部的 A / D 背光补偿电路，写一个值到这个寄存器 SCCB 没有任何效果。如果寄存器 27bit2 = 1，U 型通道偏移调整将使用寄存器可以通过 SCCB 改变。如果寄存器 26 bit1 =1，这个寄存器没有影响到 A / D 输出数据。如果输出 RGB 原始数据，该寄存器将调整的 R / G/ B 的数据。
U7: 偏移调整的方向：0 –add　U[6:0];　1Subtract　U[6:0]。
如果寄存器 2D　bit0 = 0，这个寄存器没有这个功能。

Register 23- rw: Crystal Current control.

Bits	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0
Default	0	0	0	-	-	-	-	-

CC7 - CC6: Crystal amplifier current gain. (00) maximum current; (11) minimum current
CC5 ~ CC0: Reserved

Register 24- rw: 机载预警自动曝光白色像素比

Bits	AEW7	AEW6	AEW5	AEW4	AEW3	AEW2	AEW1	AEW0
Interlace	0	0	0	0	1	0	0	0
Progressive Scan	0	0	0	1	0	0	0	0

图像亮度取决于寄存器 24 和 25 共同控制的 AEC 目标值
For a brighter image, increase register 24 and decrease register 25.

For a darker image, decrease register 24 and decrease reister 25.
AEW7-AEW0 -用于计算的白色像素比. OV7620 AEC algorithm counts the whole field/frame white pixel (its luminance level is higher than a fixed level) and black pixel (its luminance level is lower than a fixed level) number. When white/black pixel ratio is same as the ratio defined by registers [25] and [26], image stable. This register is used to define the white pixel ratio, default is 25%, each LSB represent step: Interlaced: 1.3%; Progressive Scan: 0.7%. Change range is: Interlaced: [01] ~ [4A]; Progressive Scan: [01] ~ [96]. Increase AEW<7:0> will increase the white pixel ratio. For same light condition, the image brightness will increase if AEW<7:0> increase.
Note: AEW<7:0> must combined with register [26] AEB<7:0>. Keep the relation always true: AEW<7:0> +AEB<7:0> > [4A] for Interlaced; AEW<7:0> + AEB<7:0> > [90].

Register 25- rw: AEC 自动曝光黑色像素比

Bits	AEB7	AEB6	AEB5	AEB4	AEB3	AEB2	AEB1	AEB0
Interlace	0	1	0	0	1	0	1	0
Progressive Scan	1	0	0	0	1	0	1	0

AEB7-AEB0 -用于计算的黑像素比例。OV7620 AEC algorithm is count whole field/frame white pixel (its luminance level is higher than a fixed level) and black pixel (its luminance level is lower than a fixed level) number. When white/black pixel ratio is same as the ratio defined by registers [25] and [26], image stable. This register is used to define black pixel ratio, 原始数据是75%, each LSB represent step:隔行: 1.3%; 逐行扫描: 0.7%。改变的范围是:
隔行扫描: [01] ~ [4A];逐行扫描: [01] ~ [96]. 增加 AEB<7:0> 将增加黑色像素比
.。在相同的光照条件,图像亮度将下降 如果 AEB<7:0> 增加。
注意: AEB<7:0> 必须和register [25] AEW<7:0>结合。始终保持: AEW<7:0> +
AEB<7:0> > [4D] for 隔行扫描; AEW<7:0> + AEB<7:0> > [90].

Register 26 - rw: Common control F

Bits	COMF7	COMF6	COMF5	COMF4	COMF3	COMF2	COMF1	COMF0
Default	1	0	1	0	0	0	1	0

COMF7 - COMF6: 数码锐度阈值选取。
[00] -相邻像素的亮度差异大于 8 mV 时，校正。
[01] - 16 mV.
[10] - 32 mV.
[11] - 64 mV.
COMF5 - COMF4: 数字清晰度震级的选择。
[01] –强度是相邻的 50％像素的亮度差异。
[10] - 100%.

[11] - 200%.

COMF3 - Reserved

COMF2 -交换总线 MSB/ LSB。“1” LSB->Bit7, MSB->Bit0; “0” 正常。

COMF1 - “1” A / D 黑电平校正启用。 不用“0”.

COMF0 - “1” 输出的前 4 行的黑电平隔行扫描模式和 8 行逐行扫描黑电平模式在输出有效数据前。HREF 会相对增加 4 / 8。 “0” 无黑电平输出。

Register 27 - rw: Common control G

Bits	COMG7	COMG6	COMG5	COMG4	COMG3	COMG2	COMG1	COMG0
Default	1	1	1	0	0	0	1	0

COMG7: Reserved.

COMG6: Reserved.

COMG5: Reserved.

COMG4: RGB 矩阵禁用. “1” - Bypass RGB matrix. “0” – 启动RGB matrix.

COMG3: Reserved.

COMG2: “1” Enables manual adjustment of A/D offset: 1 - A/D data will add or subtract a value defined by registers [21] and [22]. 0 - A/D data will be shifted by a value defined by registers [21], [22] and [2E], which is updated by internal circuit.

COMG1: - Disables CCIR range clip.

COMG0: - Special interface for external micro-controller and RAM timing control. See timing chart.

Register 28 - rw: Common control H

Bits	COMH7	COMH6	COMH5	COMH4	COMH3	COMH2	COMH1	COMH0
Default	0	0	0	0	0	0	0	0

COMH6: - “1” 使能黑/白模式。

COMH5: - “**1“选择逐行扫描模式，“0“选择隔行扫描模式。**

COMH4: - Freeze AEC/AGC value - current values retained. This is effective only when register 13 bit 0=1.

COMH3: - AGC disable.

COMH2: -原始数据输出格式：“1” - Green on Y channel, B R B R....on UV channel (GRB422), “0” – G R G R.... on Y channel, B G B G..... on UV channel.

Register 29 - rw: Common control I

Bits	COMI7	COMI6	COMI5	COMI4	COMI3	COMI2	COMI1	COMI0
Default	0	0	0	0	0	0	0	0

COMI7: - AEC 禁用. “1” 如果寄存器 13 bit 0=1, AEC 停止并且寄存器 [10] 的值将被保持在最后的 AEC 的值并且不是由内部电路进行更新。
“0 “ - 如果寄存器 13bit0 = 1，寄存器[10]的值将由内部电路进行更新。
COMI6: - 使能从机模式选择。“1”从机模式，使用外部 CHSYNC 和 VSYNC。
“0” 主机模式。
COMI<5:4> - Reserved.
COMI3: - 中央加权曝光控制。
COMI2: - Reserved.
COMI1 - COMI0: 版本标志

Register [2A] - rw: Frame Rate Adjust Register 1

Bits	EHSH7	EHSH6	EHSH5	EHSH4	EHSH3	EHSH2	EHSH1	EHSH0
Default	0	0	0	0	0	0	0	0

EHSH7 -帧速率的调整使能位。 “1 “启用。

EHSH<6:5> -最高的 2 位的帧速率调整控制字节。 见解释 寄存器[2B]。
EHSH4 - “1” - UV component 延迟2个像素。“ 0” no 2*Tp delay.
EHSH3 - Y 通道亮度调节使能。当 COMF2= 1 active。
EHSH2 -对于 QVGA 格式的原始数据。 “1”将迫使 Y 的输出 BGBG 和 U V 输出 GRGR。
EHSH<1:0> - Reserved.

Register [2B] - rw:帧频调整寄存器 2

Bits	EHSL7	EHSL6	EHSL5	EHSL4	EHSL3	EHSL2	EHSL1	EHSL0
Default	0	0	0	0	0	0	0	0

EHSL<7:0> -最低为 8 位的帧速率调整控制字节。帧频调整分辨率为 0.12%。
控制字为 10 位。每计数下降 0.12%的帧速率。范围为 0.12% -112%。如果启用调整帧速率，COME7 必须设置为“0”。

Register [2C] - rw: Black Expanding Register

Bits	EXBK7	EXBK6	EXBK5	EXBK4	EXBK3	EXBK2	EXBK1	EXBK0
Default	1	0	0	0	1	0	0	0

EXBK<7:4> - 粗自动黑电平调整。范围是 0.08％- 1.3％
EXBK<3:0> -精细自动黑电平调整。范围是 0.08％- 1.3％。

Register [2D] - rw: Common Control J

Bits	COMJ7	COMJ6	COMJ5	OMJ4	COMJ3	COMJ2	COMJ1	COMJ0
Default	1	0	0	0	0	0	-	1

COMJ7- 保留。始终设置为“1 “。
COMJ6-**QVGA 的 60 帧/ s 的选择。 “1 “只有在隔行扫描模式奇数据输出领域， “0 “奇/偶场数据输出帧率为 30 帧/秒。VGA 是输出每秒 60 帧的双行模式的原始数据/秒。**
COMJ5- 保留。始终设置为“0 “。
COMJ4- 自动亮度启用。
COMJ3- 保留。始终设置为“0 “。
COMJ2-捆扎过滤器使能。经过调整帧速率，以配合室内的光的频率，该位使不同曝光算法减少光带荧光光致。
COMJ1- 保留。始终设置为“0 “。
COMJ0- 保留。始终设置为 “

Register [2E]- rw: V Channel Offset Adjustment

Bits	V7	V6	V5	V4	V3	V2	V1	V0
Default	1	0	0	0	0	0	0	0

V7 的- V0 标准：V 通道数字输出偏移调整。范围:+128 毫伏～-128mV。如果 COMG2=0 时，该寄存器将自动更新内部的 A / D 背光补偿电路，写一个值到这个 SCCB 寄存器没有任何效果。如果 COMG2= 1，V 通道偏移调整将使用寄存器中的值它可以改变 SCCB。如果 COMF1=1，该寄存器没有到 A / D 输出数据的影响。如果输出原始数据，该寄存器将调整的 R / G/ B 的数据。

V7 的：胶印调整方向：o - Add V[6:0]; 0-Substrate V[6:0].如果 COMJ0=0 时，该寄存器的值是常见的 U 和 V 通道。

Register 2F ~ 5F - w: Reserved

Address [2F] - [5F] are reserved for internal use.

Register 60- rw: Signal Process Control A

Bits	SPCA7	SPCA6	SPCA5	SPCA4	SPCA3	SPCA2	SPCA1	SPCA0
Default	0	0	1	0	0	1	1	1

SPCA7: 增益提升 1.5 倍。
SPCA6: Reserved.
SPCA5: “1” disables green averaging for UV channel.
SPCA4: “1” disables green averaging for lumninance channel.
SPCA<3:2> Reserved.
SPCA<1:0>: Reserved. Color set to “0111”; B&W set to “0000”.

Register 61- rw: Signal Process Control B

Bits	SPCB7	SPCB6	SPCB5	SPCB4	SPCB3	SPCB2	SPCB1	SPCB0
Default	1	0	0	0	0	0	1	0

SPCB7: “1” YUV mode; “0” raw data mode.
SPCB6: Reserved. Always set to “0”.
SPCB5: Reserved. Always set to “0”.
SPCB4: Reserved. Always set to “0”.
SPCB3: Reserved. Always set to “0”.
SPCB2: Limits range of register [6] to half value.
SPCB<1:0>:自动亮度指标参考电平：（00） - 0 IRE ;（01） - 6IRE （10） - 10 IRE （11） - 20 的 IRE。

Register 62- rw: RGB Gamma Control

Bits	RGM7	RGM6	RGM5	RGM4	RGM3	RGM2	RGM1	RGM0
Default	0	0	0	1	0	0	1	0

RGM<7:1> raw data or UV gamma curve selection.
RGM0: Reserved. Always set to “0”.

原始数据或 UV gamma 曲线的选择。

Register 63- rw: Reserved

Address [63] are reserved for internal use.

Register 64- rw: Y Gamma Control

Bits	YGM7	YGM6	YGM5	YGM4	YGM3	YGM2	YGM1	YGM0
Default	0	1	0	1	1	0	0	1

YGM<7:1>: Y gamma curve selection.
YGM<0>: "1" enable; "0" disable (linear).

Register 65- rw: Signal Process Control C

Bits	SPCC7	SPCC6	SPCC5	SPCC4	SPCC3	SPCC2	SPCC1	SPCC0
Default	0	1	0	0	0	0	1	0

SPCC<7:3> Reserved.
SPCC2: A / D 转换模式的选择。增加 1.5 倍的 A / D 范围
SPCC<1:0>: A / D 参考选择。 <00>：输入信号范围为 0.9V;<01>：1.0V 的峰值
“10>：1.15V 的峰值 1>：1.26V 的峰值。不要使用<00>.

Register 66- rw: AWB Process Control

Bits	AWBC7	AWBC6	AWBC5	AWBC4	AWBC3	AWBC2	AWBC1	AWBC0
Default	0	1	0	1	0	1	0	1

YUV 的矩阵控制。

Register 74:7 must be enabled for AWB process control.
AWBC<7:6>: Smart AWB ignores RGB raw data pixel values above (00):70%, (01): 80%, (10): 90%,
(11):100%.
AWBC<5:4>: Smart AWB ignores RGB raw data pixel values below (00):10%, (01) 20%, (10) 30%,
(11) 40%.
AWBC<3:2>: U threshold level selection if use U/V as white balance feedback

00: (-10% ~ 10%); 01: (-20% ~ 20%); 10: (-30% ~ 30%); 11: (-40% ~ 40%)
AWBC<1:0>: V threshold level selection if use U/V as white balance feedback

00: (-10% ~ 10%); 01: (-20% ~ 20%); 10: (-30% ~ 30%); 11: (-40% ~ 40%)

Register 67- rw: Color Space Selection

Bits	YUV7	YUV6	YUV5	YUV4	YUV3	YUV2	YUV1	YUV0
Default	0	0	0	1	1	0	1	0

YUV<7:6>:
- [00]: YUV
- [01]: Analog YUV
- [10]: CCIR 601 YCrCb
- [11]: PAL YUV

YUV5: U/V 信号延迟 2 像素的选择
YUV<3:2>:信号延迟的选择(00) - 0; (01) - 1; (10) - 2; (11) - 3 像素

Register 68- rw: Signal Process Control D

Bits	SPCD7	SPCD6	SPCD5	SPCD4	SPCD3	SPCD2	SPCD1	SPCD0
Default	1	1	0	0	1	1	0	0

SPCD<7:5>: AEC/AGC Brighness Target level selection.
000 - 10%; 001 - 30%; 010 - 50%; 011 - 70%; 100 - 80%; 101 - 90%; 110 - 100%; 111 - 110%.
SPCD4: Reserved. Always set to “0”.
SPCD<3:2>: Anti-alias threshold: 11 最低门槛；, 10 中档门槛；00 最高的门槛。
SPCD<1:0>: Anti-alias magnitude: 00 -低强度；1, 10 中强度； 11: 高强度。

Register 69- rw: Analog Sharpness

Bits	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0
Default	0	1	1	1	0	0	1	0

EDGE<7:3> Reserved.
EDGE2: Vertical Edge Enhancement enable. Register 20:5 must be set to “1”.
EDGE<1:0>: Reserved.

Register 6A- rw: 垂直边缘增强控制

Bits	VEG7	VEG6	VEG5	VEG4	VEG3	VEG2	VEG1	VEG0
Default	-	1	0	0	0	0	1	0

VEG<6:4>: Vertical Edge Enhancement threshold range
VEG<3:0>: Vertical Edge Enhancement magnitude value. 0000: weakest; 1111: strongest.

Register 6B-6E rw: Reserved

Address [6B] - [6E] are reserved for internal use.

Register 6F - rw:奇偶噪声补偿控制

Bits	EOC7	EOC6	EOC5	EOC4	EOC3	EOC2	EOC1	EOC0
Default	-	-	1	1	1	0	1	0

EOC<7:6>: Reserved.
EOC<5:4>: Color Kill luminance threshold selection: 00 - none; 01 - 2.6v; 10 - 2.4v; 11 - 2.3v. Lower luminanceselection will activate color kill.
EOC<3:0>:到出厂设置的推荐值。

Register 70 - rw: Common Control K

Bits	COMK7	COMK6	COMK5	COMK4	COMK3	COMK2	COMK1	COMK0
Default	1	0	0	0	0	0	0	1

COMK7 - “1” 的 HREF 和 PCLK 的边缘重合负/下降沿（无延迟）（COMD6 必须设置为“0“）。 “0“的 HREF 边沿发生后 10 PCLK 的正/上升沿纳秒。
COMK6 - Output port drive current additional 2x control bit.
COMK5 - Reserved.
COMK4 - Selects ZV port timing. “1” VSYNC output ZV port vertical sync signal。“0” 正常 TV 垂直同步信号。
COMK3 - Accelerated saturation mode for camera mode change. (QVGA, 8 Bit output, CCIR 656 mode and Progressive Scan Mode). After relative control bit set, the first VS will be the stable image with suitable AEC/AWB setting. “0” - slow mode, after mode change need more field/frame to
get stable AEC/AWB setting image.
COMK2 - Reserved.
COMK1 - AWB update rate selection. “1” fast mode; “0” slow mode.
COMK0 - Set to “1” in single line mode, otherwise set to “0” and set COMG4 to disable.

Register 71 - rw: Common Control J

Bits	COML7	COML6	COML5	COML4	COML3	COMK2	COML1	COML0
Default	0	0	0	0	0	0	0	0

COML7 -自动亮度更新率: “1” - Slow mode; “0” - fast mode.
COML6 - Gated PCLK selection. “1” - Enables PCLK gated by HREF; “0” - PCLK is free running clock
COML5 - Swap HREF output pin with CHSYNC. “1” - HREF pin output CHSYNC signal; “0” - No swap.
COML4 - Swap CHSYNC output pin with HREF. “1” - CHSYNC pin output HREF signal; “0” - normal output.
COML<3:2>- Highest 2 bit for HSYNC rising edge shift control, combined with register [72]
COML<1:0>- Highest 2 bit for HSYNC falling edge shift control, combined with register [73]

Register 72- rw: Horizontal Sync 1st Edge shifting

Bits	HSDY7	HSDY6	HSDy5	HSDY4	HSDY3	HSDY2	HSDY1	HSDY0
Default	0	0	0	1	0	1	0	0

HSDY<7:0> - Lower 8 bit control for shifting horizontal sync CHSYNC first edge. Range is [000] - [3FF].
Every count equals 1 PCLK.

Register 73 - rw: Horizontal Sync 2nd Edge shifting

Bits	HEDY7	HEDY6	HEDY5	HEDY4	HEDY3	HEDY2	HEDY1	HEDY0
Default	0	1	0	1	0	1	0	0

HSDY<7:0> - Lower 8 bit control for shifting horizontal sync CHSYNC second edge. Range is [000] - [3FF].
Every count equals 1 PCLK.

Register 74 - rw: Common Control M

Bits	COMM7	COMM6	COMM5	COMM4	COMM3	COMM2	COMM1	COMM0
Default	0	0	1	0	0	0	0	0

COMM7 - Enable UV Smart AWB threshold control.

COMM<6:5> - AGC maximum gain selection: 00 - 2x; 01 - 4x; 10 - 2x; 11 - 8x
COMM<4:0> - Reserved.

Register 75 - rw: Common Control N

Bits	COMN7	COMN6	COMN5	COMN4	COMN3	COMN2	COMN1	COMN0
Default	1	0	0	0	0	0	1	0

COMN7 - “1” enables Auto brightness range limit. Minimum will be [40]. Otherwise will be [00] ~ [FF].
COMN<6:3> - Reserved.
COMN2 - This bit further reduces the exposure time to 1/120 second or 1/100 second when the banding filter
is enabled and the light is too strong.
COMN1- If enabled, manual write white balance value, then change to auto, the stable time will be less.
Speeds white balance stable time when switching from manual to AWB.
COMN0 - Enables addition of 2 pixel averaging.

Register 76 - rw: Common Control O

Bits	COMO7	COMO6	COMO5	COMO4	COMO3	COMO2	COMO1	COMO0
Default	0	0	0	0	0	0	0	0

COMO7 - Output XCLK from **FODD** pin.
COMO6 - Reserved.
COMO5 - Software power down enable: 1 - enable; 0 - wake up
COMO4 - Reserved.
COMO3 - Limits the Minimum Exposure time to 4 lines rather 1 line with AEC enable
COMO2 - Tri-state sync and CLK output, except data line
COMO<1:0> - Reserved.

Register 77-7B - rw: Reserved

Address [2F] - [5F] are reserved for internal use.

Register 7C - rw: Field Average Level Storage

Bits	AVG7	AVG6	AVG5	AVG4	AVG3	AVG2	AVG1	AVG0
Default	0	0	0	0	0	0	0	0

AVG<7:0> -- Strorage fileld luminance average value if register 20 bit 6=1.
Notice: for QVGA and Progressive Scan mode, the real luminance average value is double of this register value, other mode is same. If set to RGB raw data mode, the value is Green component average value.